

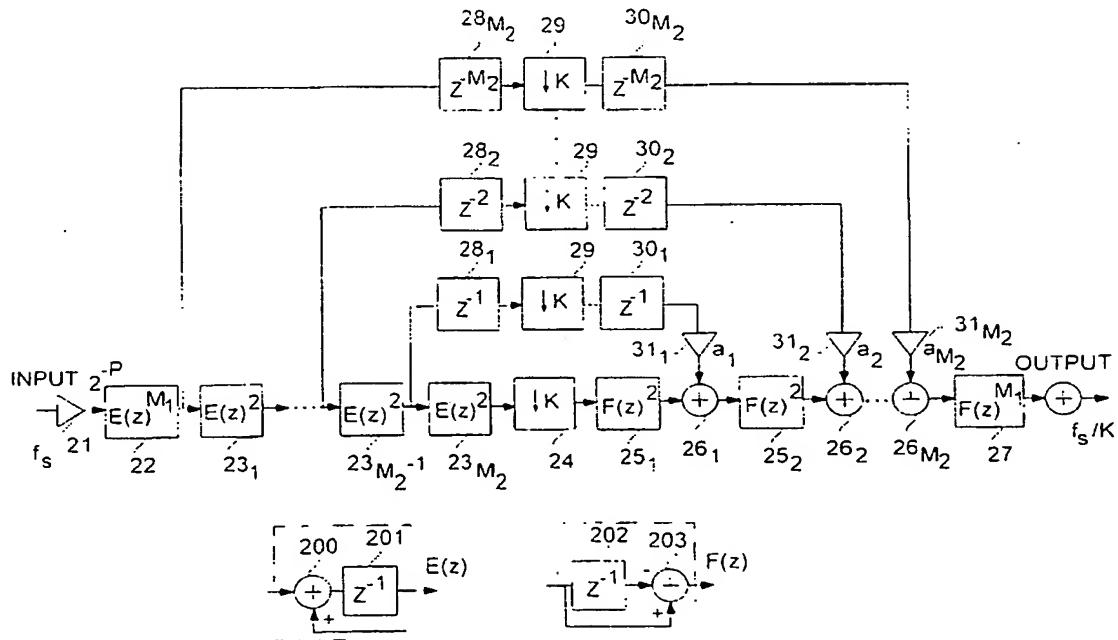


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(71)(72) Applicants and Inventors: SARAMÄKI, Tapio [FI/FI]; Kreetaninkuja 4 A, FIN-33950 Pirkkala (FI). RITONIEMI, Tapani [FI/FI]; Insinöörinkatu 84 B 31, FIN-33720 Tampere (FI). EEROLA, Ville [FI/FI]; Tohlopinkatu 15 A 2, FIN-33310 Tampere (FI). HUSU, Timo [FI/FI]; Kirkkokatu 12 B 23, FIN-80110 Joensuu (FI). PAJARRE, Eero [FI/FI]; Kanjoninkatu 11 C 26, FIN-33720 Tampere (FI). INGALSUO, Seppo [FI/FI]; Orivedenkatu 8 C 66, FIN-33720 Tampere (FI).		
(74) Agent: OY KOLSTER AB: Iso Roobertinkatu 23, P.O. Box 148, FIN-00121 Helsinki (FI).		

(54) Title: DECIMATION FILTER



(57) Abstract

The invention relates to a decimation filter comprising a direct cascade arrangement of digital first order and second order integration and derivation stages (22, 23, 25, 27) and a decimation stage. The decimation filter structure of the invention comprises additional branches (28, 29, 30, 31) for shifting the location of the attenuation zeros of the decimation filter and thereby reducing the order M and the number of structural elements M of the required filter.

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Decimation filter

The present invention relates to a decimation filter comprising a cascade arrangement of the following elements in the given order:

M₁ digital first order integration stages having a clock rate F_s and a delay of one clock cycle,

M₂ digital second order integration stages having a clock rate F_s and a delay of two clock cycles,

a decimation stage for decreasing the sampling frequency of the output signal from the last integration stage by a predetermined decimation ratio K,

M digital derivation stages having a clock rate F_s/K, each comprising a delay element stage for delaying the input signal for one clock cycle and a subtractor element stage for subtracting the input signal from the output signal of the delay element, wherein M=M₁+2M₂.

A decimation filter is a digital filter whereby the sampling frequency of a signal is decreased (decimated) by a number K (normally an integer) which is called the decimation ratio. A decimation filter is typically used in connection with an oversampling A/D or D/A converter (e.g. sigma-delta converter) to decrease the output sampling frequency of the converter.

Decimation can in principle be performed in one stage comprising a low-pass filter and a unit taking every K:th sample from the output of the low-pass filter, K being the decimation ratio. The filtering response of the low-pass filter must be such that the information carried by the output signal of the filter fits into the band according to the new sampling frequency. A problem attendant the decimation carried out in one stage will be that a low-pass filter

having a very steep and narrow-band frequency response is needed. This problem has traditionally been overcome by performing the filtering and decimation in several stages, so that the product of the decimation ratios K_1, K_2, \dots, K_n of the different decimation stages is the requisite decimation ratio K stated above. Thus the requirements on the characteristics of the low-pass filters required in the individual stages are relieved and their number of order is decreased so that the overall number of order in the low-pass filters of the different stages is only a fraction of that of a corresponding single-stage implementation. This is particularly the case when the decimation ratio M is high, e.g. > 50 .

The computationally efficient first stage for multistage decimators is provided by a transfer function

$$H(z) = 2^{-p} \left[\frac{1-z^{-K}}{1-z^{-1}} \right]^M ,$$

20

where 2^{-p} is a scaling constant. It can be used as a first stage with decimation factor K in cases where the overall decimation factor D can be realized in the product

25

$$D = KL,$$

30 where K and L are integers. The design and structure of such a filter have been described for instance in the article E.B. Hogenauer, "An economical class of digital filters for decimation and interpolation", in IEEE

Trans. Acoust. Speech Signal Processing, pp. 155-162, vol. ASSP-29, April 1981. One known decimator structure satisfying the transfer function according to equation 1 is shown in Figure 1. The decimator requires only $2M$ adders and $2M$ delay elements and no multiplying operations. Furthermore, Figure 1 shows a scaling element 12 and a decimation block 13 forwarding only every K :th sample. It should be noted that if 1's or 2's complement arithmetic (or modulo arithmetic in general) and the worst-case scaling are used, the output values of a filter $H(z)$ implemented as shown in Figure 1 are correct even though internal overflows were to occur in the feedback loops realizing the term $1/(1 - z^{-1})$. Furthermore, under the above conditions the effect of temporary miscalculations vanishes from the output in finite time and initial resetting is not necessarily needed. The scaling constant 2^{-p} has to satisfy the condition

20 $2^{-p} \leq (1/K)^M$.

The integer M for the prior art filter structure has to be selected in such a way that $H(z)$ provides the required attenuation in the frequency bands

25 $[F_s/2(2r/K - 1/D), F_s/2(2r/K+1/D)], \quad r=1, 2, \dots, [K/2]$

which alias into the frequency band $[0, F_s/2(1/D)]$ of the overall decimator. Herein F_s is the input sampling frequency. The prior art structure shown in Figure 1 is attended by the disadvantage that the zeros produced by the transfer function thereof are located at frequencies $F_s/K, 2*F_s/K, 3*F_s/K, \dots, (K-1)*F_s/K$, and the integer M can only increase their number, i.e. the number

of order of the filter. This results in that the number of structural elements in the prior art filter stage is unnecessarily high for the required attenuation at frequencies $[F_s/2(2r/K-1/D), F_s/2(2r/K+1/D)]$. A high number 5 of structural elements increases the number of additions and delays required in the implementation. However, the major disadvantage is the increase of the gain of the filter when the number of order increases, and thus the number of additional bits required in the 10 structure increases. The required number of additional bits is the smallest integer which is higher than $\log_2 K^M$.

The object of the present invention is a filter structure in which the number of structural elements can be considerably reduced in comparison with prior art structures having the same attenuations at frequencies $[F_s/2(2r/K-1/D), F_s/2(2r/K+1/D)]$. In the structure according to the invention, the necessary attenuation can be achieved with lower-order structures 15 than was previously possible, on account of the better 20 location of the attenuation zeros.

This is achieved with the decimation filter set forth in the preamble, which in accordance with the invention is characterized in that the decimation filter further comprises M_2 signal processing branches in such a way that between the input of the i :th second 25 stage integrator subsequent to the M_1 -stage integrator and the output of the derivation stage of the i :th second stage subsequent to the decimation block in the main branch a signal processing branch (realizes the $(i+K^i)$ clock cycle delay at sampling frequency F_s and the coefficient) is connected comprising, in series 30 configuration, a first delay element having a delay of i clock cycles at sampling frequency F_s of the output signal, a decimation stage for decreasing the sampling 35

frequency of the first delay element by a predetermined decimation ratio K, a second delay element having a delay of i clock cycles at sampling frequency F_s/K , and a scaling element having a scaling factor a_i where $i = 5, 2, 3, \dots, M_2$.

The present invention also relates to another decimation filter as set forth in the preamble, which is characterized in that the decimation filter comprises M_2 signal processing branches in such a way that between the input of the i :th second stage integrator subsequent to M_1 and the output of the main branch a signal processing branch is connected comprising, in series configuration, a first delay element having a delay of i clock cycles at sampling frequency F_s of the output signal, a decimation stage for decreasing the sampling frequency of the first delay element by a predetermined decimation ratio K, a second delay element having a delay of i clock cycles at sampling frequency F_s/K , a $(M_1+2(M_2-i))$ -stage derivation block, and a scaling element having a scaling factor a_i where $i = 10, 2, 3, \dots, M_2$.

The decimation filter structure according to the invention comprises additional branches for shifting the location of the attenuation zeros of the decimation filter and thereby reducing the order M and the number of structural elements M of the required filter. As an example, let us consider a case with D = 64 when a 120-dB attenuation is desired. With designs according to the invention, for K = 16 the aliased terms are attenuated more than 120 dB by using $M_1 = 2$ and $M_2 = 2$. The scaling factors a_1, a_2 of the branches can be quantized to be integers which may in some cases be selected from powers of two. Where the decimation filter of the invention is realized as an integrated circuit, the use of these additional branch coefficients in-

creases the silicon area occupation in the configuration of the integrated circuit only by 10% compared to the prior art configuration having six terms ($M=6$). Without additional branches, eight terms ($M=8$) would be required to provide the desired attenuation in the prior art solution. Such a prior art filter would further require a higher internal wordlength (8 bits more, i.e. more than 30% in excess of that of the exemplified pre-filter stage of the sigma-delta modulator which has six terms), and the number of delay elements and adders would be higher. In an integrated circuit design, the estimated saving in silicon area occupation achieved with the invention over the corresponding known solution is about 30% for the case where these filters are used as first filter stages in the decimation of a one-bit data stream from a sigma-delta modulator. The structure now disclosed has the further advantage of lower amplitude distortion within the passband, thus facilitating error correction. Furthermore, in several implementations the calculation accuracy of the prior art structure becomes too high, and thus either the speed of the circuit configurations or the clock signals in the system preclude the use of the prior art structure.

In the following the invention will be set forth in greater detail by means of illustrating embodiments with reference to the accompanying drawing, in which

Figure 1 is a block diagram illustrating a prior art decimation filter,

Figure 2 is a block diagram illustrating a decimation filter according to the invention,

Figure 3 is a block diagram illustrating another decimation filter according to the invention, and

Figures 4 and 5 show frequency responses of a prior art filter and a filter according to the invention.

Reference will now be made to Figure 2, illustrating a decimation filter stage according to the invention. This decimation filter stage decreases the sampling frequency F_s of a signal applied to the input IN, said signal preferably being a one-bit data stream from a sigma-delta modulator, so that the sampling frequency of the data stream at the output OUT of the filter is F_s/K . Factor K is called the decimation ratio. At the input of the filter, a scaling element 21 having a scaling factor 2^{-p} is first provided. Subsequent to the scaling element 21, an integration block $E(z)^{M_1}$ comprising in series configuration M_1 integration stages $E(z)$ as shown in Figure 2A is connected in series.

In Figure 2A, the integration stage $E(z)$ comprises a series connection of adder 200 and delay means 201. The input signal of the integration stage is applied to one input of the adder 201, and the output signal of the delay means 201, which at the same time provides the output signal of the entire integration stage, is fed back to the second input of the adder 200. The added signal obtained at the output of the adder 200 is applied to the delay means 201.

In Figure 2, subsequent to the integration block $E(z)^{M_1}$, a series connection of M_2 second order integration blocks $E(z)^2$ is provided. Each of these blocks comprises in series configuration two integration stages as shown in Figure 2A. After the last integration stage $E(z)^2$, denoted by reference 23_{M_2} , a decimation block 24 is connected which forwards every K:th sample from the output of the integration stage 23_{M_2} . After the decimation block 24, M_2 second order derivation blocks $F(z)^2$, denoted with references 25₁,

25₂,...25_{M₂} respectively, are connected in series. Each second order derivation block F(z)² comprises in a series connection a pair of derivation stages F(z) shown in Figure 2B. After the second order derivation stage F(z)², a series connection of adders 26₁, 26₂,...26_{M₂} is provided ahead of the next second order block. These adders add the outputs of the blocks together with the signal from the corresponding branch prior to application to the next block. After the last derivation stage 25_{M₂} and adder 26_{M₂}, a derivation block F(z)^{M₁}, comprising in series configuration M₁ derivation stages as shown in Figure 2B, is connected in series.

The derivation stage F(z) of Figure 2B comprises a series connection of delay means 202 and subtractor 203. The input signal is applied to adder 203 both directly and via delay means 202 having a delay of one clock cycle, and the differential signal is applied to the output of the stage.

The decimation filter further comprises M₂ signal processing branches in such a way that between the input of the i:th second order integrator after the M₁-stage integrator and the output of the i:th second order derivation stage F(z)² after the decimation block 24 of the main branch a signal processing branch is connected which comprises, in series configuration, a first delay element 28 having a delay of i clock cycles at sampling frequency F_s of the output signal, a decimation stage 29, corresponding to decimation stage 24, for decreasing the sampling frequency of the first delay element by a predetermined decimation ratio K, a second delay element 30 having a delay of i clock cycles at sampling frequency F_s/K, and a scaling element 31 having a scaling factor α_i where i = 1,2,3,...,M₂. Thus for example from the input of integration stage 23_{M₂}-1, there is an outgoing feedforward signal process-

ing branch comprising a delay means 28₂ having a delay z^{-2} of two clock cycles at clock rate F_s , a decimation stage 29, a delay means 30₂ having a delay z^{-2} of two clock cycles at clock rate F_s/K , and a scaling element 31₂ having a scaling factor A_2 . The output of each scaling element 31₁, 31₂, ..., 31_{M₂} is coupled to the second input of the corresponding adder 26₁, 26₂, ..., 26_{M₂}.

The overall transfer function of the filter of Figure 2 is

10

$$H(z) = 2^{-K} \left[z^{-1} \frac{1-z^{-K}}{1-z^{-1}} \right]^{M_1} \left[\left[z^{-1} \frac{1-z^{-K}}{1-z^{-1}} \right]^{2M_2} + \sum_{i=1}^{M_2} a_i z^{-i(K+1)} \left[z^{-1} \frac{1-z^{-K}}{1-z^{-1}} \right]^{2(M_2-i)} \right]$$

Another alternative filter structure for realizing the above transfer function is shown in Figure 3. In Figure 3, blocks and elements that are the same as in Figure 2 have been denoted with the same references and symbols. As in Figure 2, also in Figure 3 the arrangement comprises - starting from the input IN and in the following sequence - a series connection of a scaling element 21, an M₁-stage integration block 22, M₂ second order integration blocks 23₁, ..., 23_{M₂} and a decimation block 24. After the decimation stage 24, a derivation block 25' is connected comprising in a series connection M₂ derivation blocks F(z) as shown in Figure 2B, a derivation block 27 comprising in a series connection M₁ derivation stages F(z), and an adder 33.

The decimation filter of Figure 3 further comprises M₂ signal processing branches in such a way that between the input of the i:th second stage integrator 23 after M₁ and the adder 33 in the output of the main branch a signal processing branch is connected which

comprises, in a series connection, a first delay element 28 having a delay of i clock cycles at sampling frequency F_s of the output signal, a decimation stage 29, corresponding to decimation stage 24, for decreasing the sampling frequency of the output signal of the first delay element by a predetermined decimation ratio K , a second delay element 30 having a delay of i clock cycles at sampling frequency F_s/K , an $(M_1 + 2(M_2-i))$ -stage derivation block 32, and a scaling element 31 having a scaling factor a_i where $i = 1, 2, 3, \dots, M_2$. Thus for example from the input of the second order integrator 23_{M_2-1} , there is an outgoing feedforward signal processing branch comprising a delay means 28₂ having a delay of two clock cycles at clock rate F_s , a decimation stage 29, a delay means 30₂ having a delay of two clock cycles at clock rate F_s/K , a derivation block 32₂ comprising $(M-4)$ derivation stages $F(z)$, and a scaling element 31₂ having a scaling factor A_2 .

The filter structure of Figure 2 can be used when the scaling factors a_i can be quantized to be integers. The filter structure of Figure 3 can also be used with decimal factors (fractions) a_i .

Let us next consider an exemplary case with $D = 64$ when a 120-dB attenuation is desired. For a decimation ratio $K = 16$, the aliased terms at the desired frequency bands are attenuated more than 120 dB by using $M_1 = 2$ and $M_2 = 2$. In this case, the scaling factors a_1 and a_2 can be quantized to be integers, so as to provide altogether six integration and derivation blocks (the branches are of the feedforward type). The frequency response obtained with the filter of the invention is shown by a solid line A in Figure 4. The corresponding prior art filter requires eight terms, and its response is shown by a dashed line B in Figure 4. When the decimation ratio K is increased to $K = 32$,

the prior art filter structure requires thirteen terms, whereas the proposed branched filter structure only requires eight terms. In Figure 5, the solid line A and dashed line B represent the filter responses of the
5 filter of the invention and the prior art filter, respectively.

The circuit is generally executed on silicon using parallel arithmetic in the integrator part and serial arithmetic in the derivation blocks. The
10 parallel part takes up about 3/4 of the area, owing mainly to the arithmetic (parallel adders). The proportion of the delay in the parallel part is about 15%. The integration in the decimation circuit is performed between the derivation blocks by control and a
15 parallel/series register which is very uncomplicated. The area of the serial derivation part is mostly taken up by the delays, since the arithmetic (the adder is only one-bit adder, yet the delay of one sample is equal in parallel and series configurations) is one-bit
20 arithmetic. In the structure now disclosed, the delays (delay elements) ahead of the decimation as well as the actual decimation can be realized by means of a parallel/series register and control. Only the additional delays after decimation have to be realized; mathematically all delays are present in accordance with the
25 block diagrams. This affords considerable saving in silicon area occupation. The scaling factors can be realized with an accuracy of a few bits.

The figures and the description relating to
30 them are only intended to illustrate the present invention. The decimation filter of the invention can vary in its details within the scope and spirit of the appended claims.

Claims:

1. A decimation filter comprising a cascade arrangement of the following elements in the given order:

5 M_1 digital first order integration stages having a clock rate F_s and a delay of one clock cycle,

10 M_2 digital second order integration stages having a clock rate F_2 and a delay of two clock cycles,

15 a decimation stage for decreasing the sampling frequency of the output signal from the last integration stage by a predetermined decimation ratio K ,

20 M digital derivation stages having a clock rate F_s/K , each comprising a delay element stage for delaying the input signal for one clock cycle and a subtractor element stage for subtracting the input signal from the output signal of the delay element, wherein $M=M_1+2M_2$,

25 characterized in that the decimation filter further comprises M_2 signal processing branches in such a way that between the input of the i :th second stage integrator subsequent to the M_1 -stage integrator and the output of the derivation stage of the i :th second stage subsequent to the decimation block in the main branch a signal processing branch is connected comprising, in series configuration, a first delay element having a delay of i clock cycles at sampling frequency F_s of the output signal, a decimation stage for decreasing the sampling frequency of the first delay element by a predetermined decimation ratio K , a second delay element having a delay of i clock cycles at sampling frequency F_s/K , and a scaling element having a scaling factor α_i where $i = 1, 2, 3, \dots, M_2$.

30 2. A decimation filter as claimed in claim 1, characterized in that at the input of the

decimation filter, a scaling element is provided for scaling the input signal by a factor 2^{-p} .

3. A decimation filter as claimed in claim 1 or 2, characterized in that $M_1=M_2=2$.

5 4. A decimation filter as claimed in claim 3, characterized in that the scaling factors a_{M_1} are integers.

10 5. A decimation filter comprising a cascade arrangement of the following elements in the given order:

M_1 digital first order integration stages having a clock rate F_s and a delay of one clock cycle,

M_2 digital second order integration stages having a clock rate F_2 and a delay of two clock cycles,

15 a decimation stage for decreasing the sampling frequency of the output signal from the last integration stage by a predetermined decimation ratio K ,

20 M digital derivation stages having a clock rate F_s/K , each comprising a delay element stage for delaying the input signal for one clock cycle and a subtractor element stage for subtracting the input signal from the output signal of the delay element, wherein $M=M_1+2M_2$,

25 characterized in that the decimation filter further comprises M_2 signal processing branches in such a way that between the input of the i :th second stage integrator subsequent to M_1 and the output of the main branch a signal processing branch is connected comprising, in series configuration, a first delay element having a delay of i clock cycles at sampling frequency F_s of the output signal, a decimation stage for decreasing the sampling frequency of the first delay element by a predetermined decimation ratio K , a second delay element having a delay of i clock cycles at sampling frequency F_s/K , a $(M_1+2(M_2-i))$ -stage

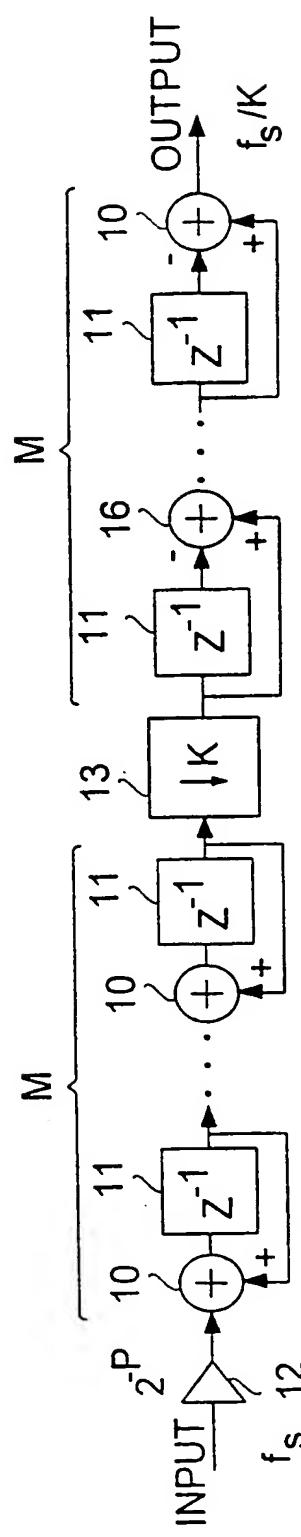
derivation block, and a scaling element having a scaling factor α_i where $i = 1, 2, 3, \dots, M_2$.

5 6. A decimation filter as claimed in claim 5, characterized in that at the input of the decimation filter, a scaling element is provided for scaling the input signal by a factor 2^{-p} .

7. A decimation filter as claimed in claim 5 or 6, characterized in that $M_1=M_2=2$.

10 8. A decimation filter as claimed in claim 7, characterized in that the scaling factors are realized with an accuracy of only a few bits.

FIG. 1



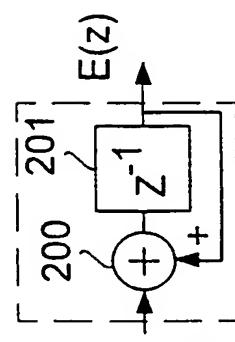
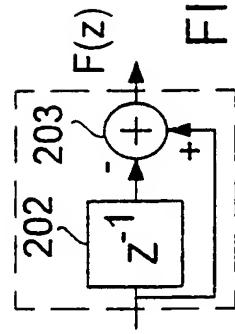
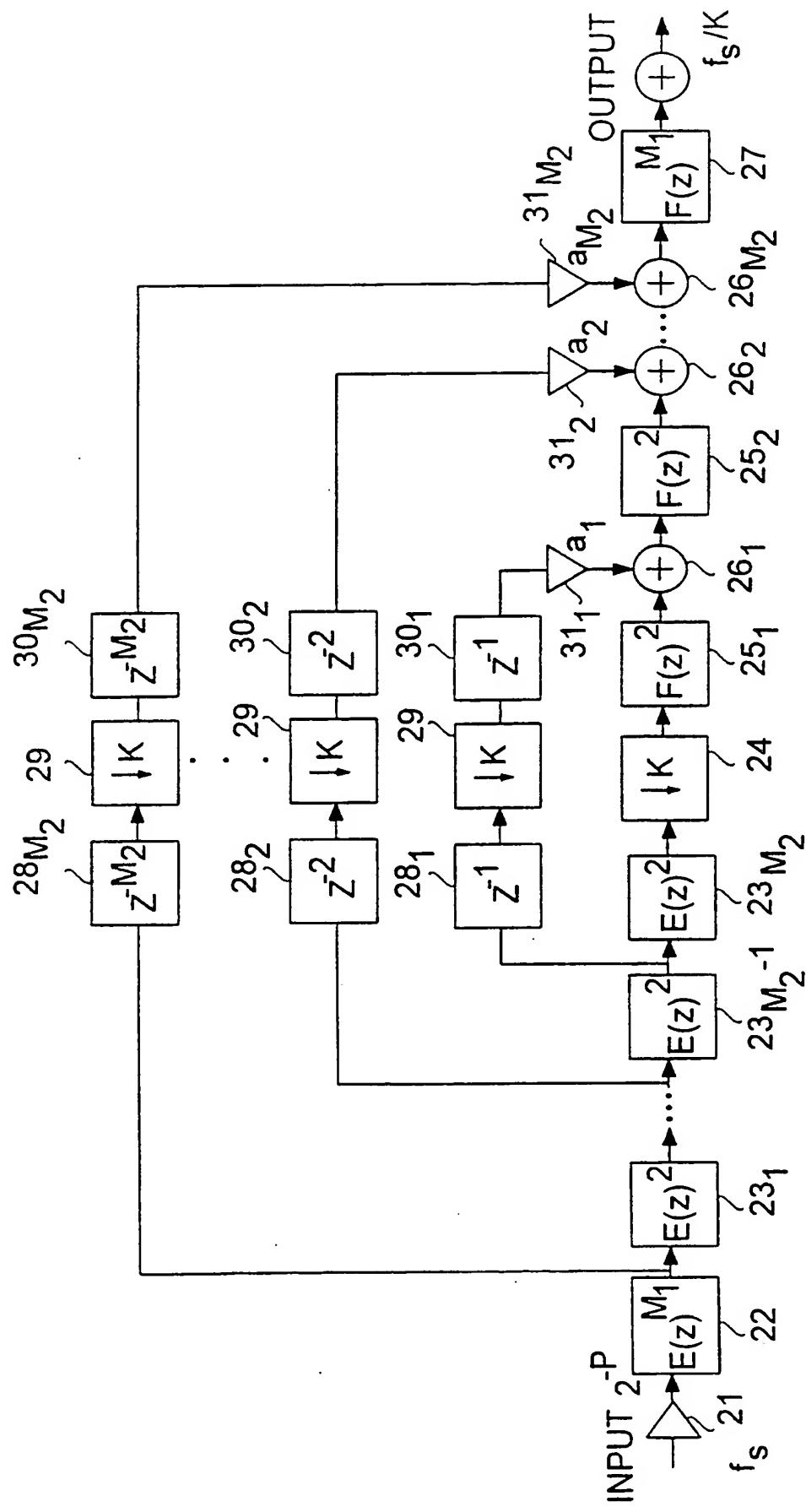


FIG. 2B

FIG. 2A

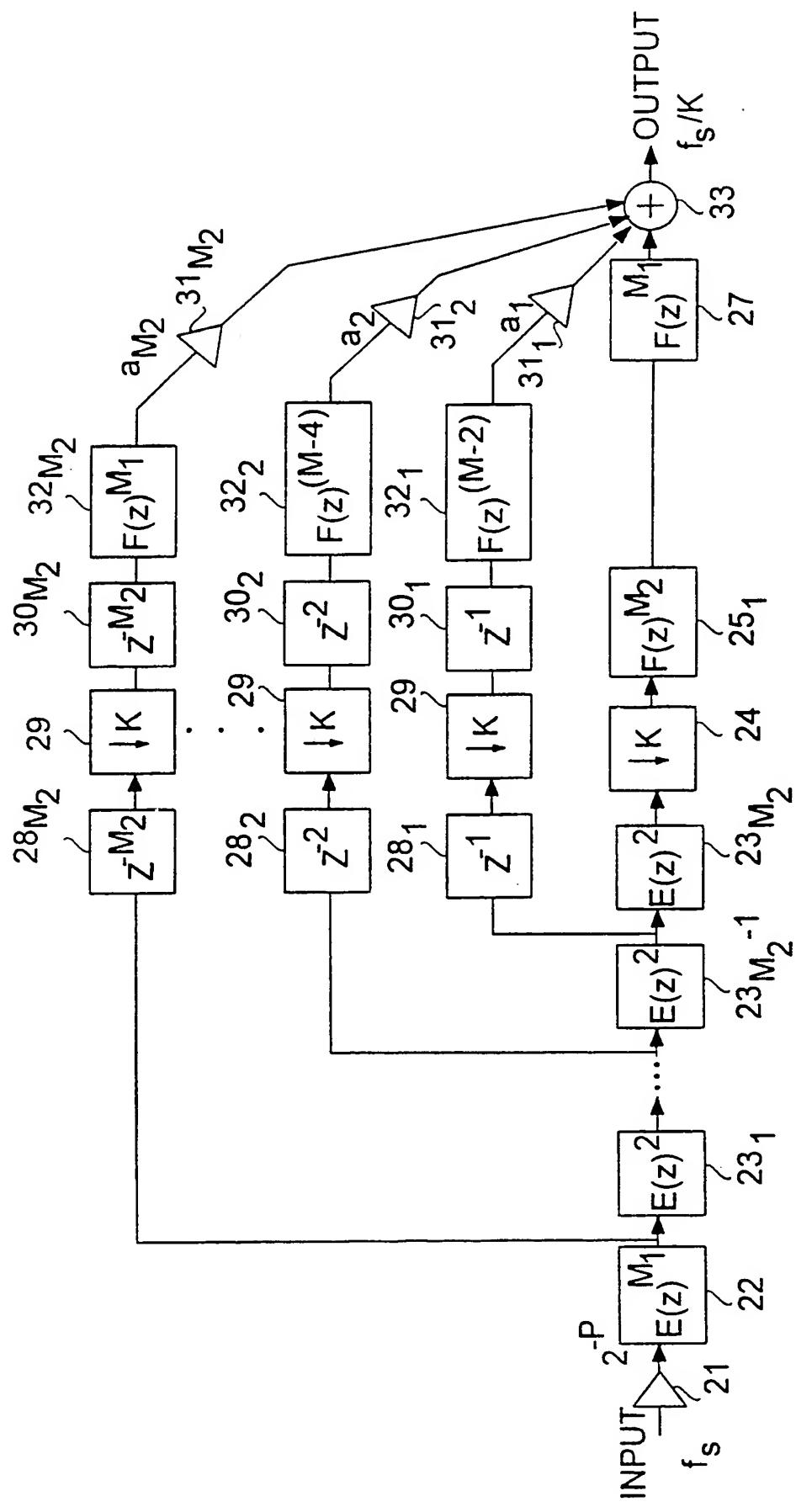
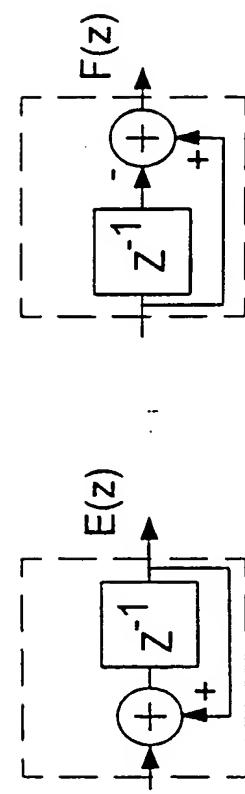


FIG. 3



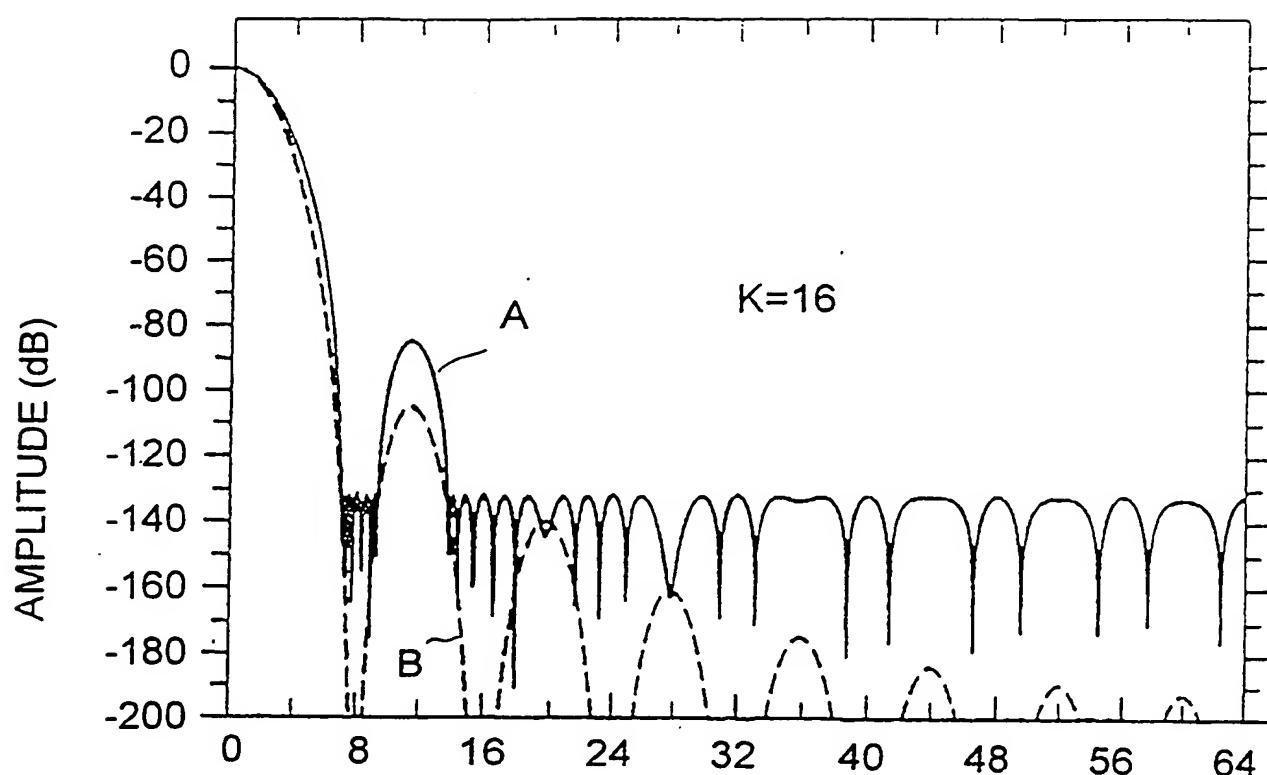


FIG. 4

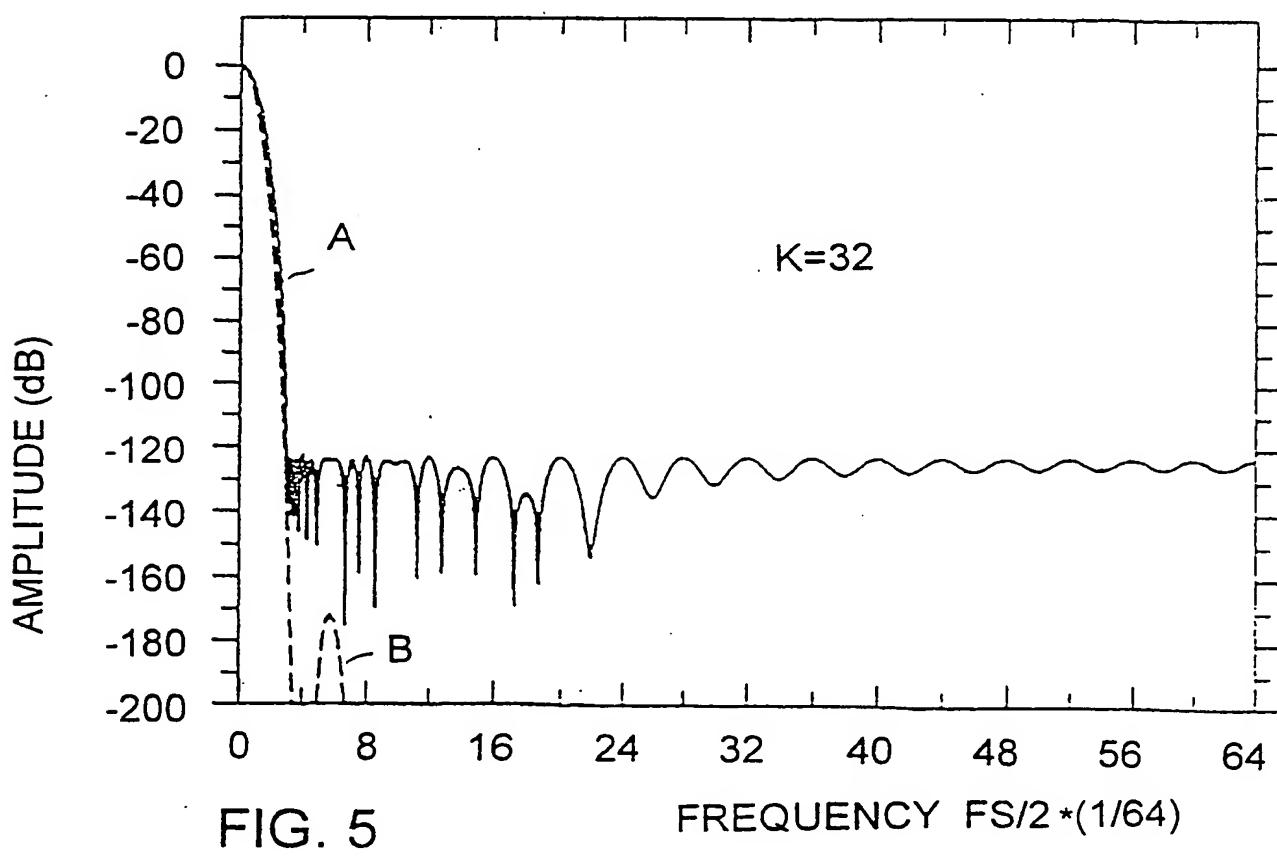


FIG. 5

INTERNATIONAL SEARCH REPORT

1

International application No.

PCT/FI 94/00125

A. CLASSIFICATION OF SUBJECT MATTER

IPC5: H03H 17/00 // G06F 15/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC5: H03H, H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4872129 (H. PFEIFER ET AL), 3 October 1989 (03.10.89), abstract, claims 1 --	1,5
A	EP, A1, 0559154 (NEC CORPORATION), 8 Sept 1993 (08.09.93), the whole document -- -----	1,5

 Further documents are listed in the continuation of Box C. See patent family annex.

- * Special categories of cited documents:
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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

02/07/94

PCT/FI 94/00125

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4872129	03/10/89	EP-A,B- 0320517	21/06/89
EP-A1- 0559154	08/09/93	NONE	